Dynamic Self-Heating Stress-Induced Degradations of Self-Aligned Top-Gate a-InGaZnO Thin-Film Transistors

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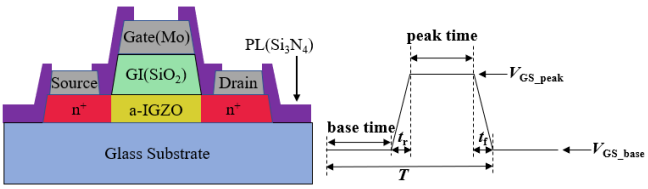
Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs), representative by a-InGaZnO (a-IGZO) TFT, have attracted extensive attention, due to high mobility, excellent uniformity, and low-fabrication temperature [1]. Recently, AOS TFTs have been gradually used in the field of circuit-driving applications, such as electroluminescence, gate driver on array (GOA) [2], and Micro-LED displays [3]. For the degradation caused by various gate bias stresses, such as positive bias temperature stress (PBTS) and negative bias illumination stress (NBIS), the AOS TFTs could suffer the threshold voltage (V_{th}) shifts (ΔV_{th}). More severe degradations will occur when the AOS TFTs suffer high-current stress under high gate bias (V_G) and drain bias (V_D).

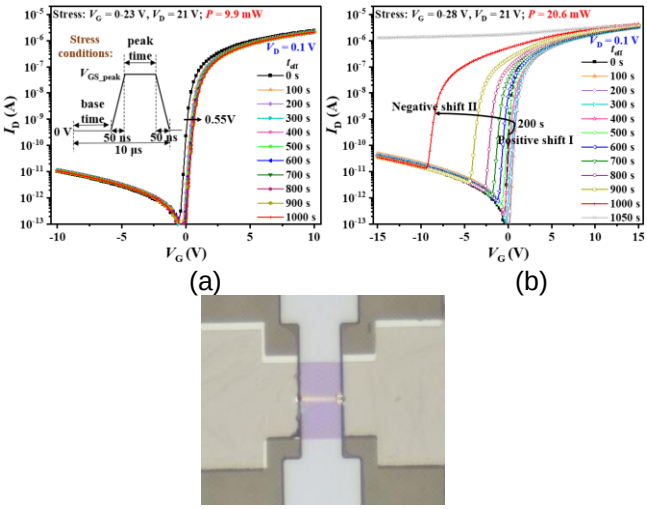
Fig. 1. (a) and (b) exhibit the schematic cross-section of a-IGZO TFT and schematic diagram of pulse gate bias stress applied in this work, respectively. Pulsed V_G and constant V_D were respectively applied to gate and drain of a-IGZO TFT to mimic practical operation conditions. The top-gate AOS TFTs have the following merits over staggered bottom-gate TFTs. Since there is no overlap between the channel and S/D, the parasitic capacitance can be reduced. The issue of device size miniaturization for bottom-gate TFTs also needs to be solved. However, when the current flows through channel, the top-gate AOS TFTs will suffer more severe thermal-induced degradations due to the poor thermal conductivities of AOSs and the channel is surrounded by gate insulator (GI) and substrate. As a crucial parameter for weighing current stress, heating power should be evaluated when the a-IGZO TFTs operate as current-driving devices.



(a) (b)

Fig. 1. (a) Schematic cross-section of a-IGZO TFT. (b) Schematic diagram of pulse gate bias stress.

The dynamic high-current stresses induced degradations of a-IGZO TFTs were evaluated. The top-gate self-aligned (TGSA) a-IGZO TFTs with 200-nm silicon nitride passivation layer (PL) were fabricated to test electrical characteristics. As shown in Fig. 2. (a), when the a-IGZO TFTs were suffered current stress with relatively low power of around 9.9 mW, the transfer curves exhibit a slightly positive shift of 0.55 V, similar to the typical degradation behavior under PBTS. The degradation mechanism can be the thermal-enhanced electrons trapped into GI. However, much more complicated degradations were observed when the current stress power reached up to 20.6 mW. The transfer characteristics first exhibit a slightly positive shift, then suffer a dramatic negative shift, and finally degrade into conductor-like curve. Due to the poor thermal conductivities of AOSs, GI, and glass substrate, the channel current will accumulate heat there and generate abundant channel donors during dynamic stress, causing negative ΔV_{th} and finally shorting the channel.



(a) (b)

(c)

Fig. 2. Evolutions of transfer curves with the effective stress time (t_{eff}) of (a) low- and (b) high-power dynamic stresses. Inset illustrates the pulse gate bias stress conditions. (c) The optical image of breakdown TFT through the glass substrate.

References

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